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APPARATUS AND METHOD FOR SAMPLE-AND-HOLD WITH BOOSTED HOLDING SWITCH

Related Application

This application claims the benefit of U.S. Provisional Application No. 60/546,706 filed February 20, 2004, the benefit of the earlier filing date of which is hereby claimed under 35 U.S.C. § 119 (e).

Field of the Invention

The invention is related to sample-and-hold circuits, and in particular, to an apparatus and method for a pipelined sample-and-hold circuit that includes a boosted hold switches that include dummies.

Background of the Invention

An analog-to-digital converter (ADC) is employed to change/convert an analog input signal into a digital output signal. There are several different types of ADCs in current use, including pipeline, flash, and folding. For pipeline ADCs, separate decoding stages are arranged in a pipeline to convert the analog signal into a digital signal.

In a flash ADC, k bits of resolution employ 2^k comparators to convert an analog signal into a digital signal. Folding ADCs are a variation of a typical flash ADC architecture except that they are arranged to map the analog input signal range into N regions where each of these N regions share the same comparators. In a folding ADC, the total number of comparators is typically $2^k/N$. Also, a folding ADC includes a coarse channel for determining from which of the N input regions the analog input signal originated. Usually, the coarse channel is configured to use coarse reference voltages that are spaced according to the voltage spacing between each folded region.

An ADC may employ a sample-and-hold circuit to relax the timing requirements of the ADC.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings, in which:

FIGURE 1 shows a block diagram of a circuit for sampling and holding;

FIGURE 2 illustrates a block diagram of an embodiment of the circuit of FIGURE 1 that includes buffer circuits;

FIGURE 3 shows a timing diagram of waveforms of embodiments of signals from the circuit of FIGURE 2;

FIGURE 4 illustrates a block diagram of an embodiment of a circuit for sampling and holding that includes a boost circuit;

FIGURE 5 shows a block diagram of an embodiment of a portion of the circuit of FIGURE 4, in which one embodiment of a hold circuit from FIGURE 4 is schematically illustrated;

FIGURE 6 illustrates a timing diagram of waveforms of embodiments of signals from FIGURE 5;

FIGURE 7 shows a block diagram of another embodiment of the portion of the sample-and-hold circuit from FIGURE 4, in which another embodiment of the hold circuit from FIGURE 4 is schematically illustrated;

FIGURE 8 illustrates a timing diagram of waveforms of embodiments of signals from FIGURE 7;

FIGURE 9 shows a block diagram of an embodiment of the circuit of FIGURE 4 that is pipelined and differential;

FIGURE 10 schematically illustrates an embodiment of a half-switch circuit from FIGURE 7; and

FIGURE 11 schematically illustrates an embodiment of a boost switch circuit from FIGURE 10, arranged in accordance with aspects of the present invention.

Detailed Description

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached

hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, and the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The phrase "in one embodiment," as used herein does not necessarily refer to the same embodiment, although it may. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to a pipelined sample-and-hold circuit. The circuit is pipelined such that processing of a held signal can continue into the next sample phase. Also, the pipelined sample-and-hold circuit includes a hold switch. The hold switch includes a boosted switch circuit and dummy circuits. The boosted switch circuit is responsive to a boosted signal. The dummy circuits are arranged for charge injection cancellation responsive to another boosted signal that is a substantially inverse of the boosted signal.

FIGURE 1 shows a block diagram of circuit 100. Circuit 100 may include sample-and-hold circuit 102 and processing circuit 120. Processing circuit 120 may be interleaved such that it includes first channel 121 and second channel 122. Similarly, sample-and-hold circuit 102 may be interleaved such that it includes sample-and-hold channel 111 and sample-and-hold channel 112. Sample-and-hold channel 111 includes sampling switch circuit S_{s1}, capacitor circuit C_{s1}, and holding switch circuit S_{h1}. Similarly, sample-and-hold channel 112 includes sampling switch circuit S_{s2}, capacitor circuit C_{s2}, and holding switch circuit S_{h2}.

In operation, during a sample phase for sample-and-hold channel 111, sampling switch circuit S_{s1} is closed and switch circuit S_{h1} is open. During the sample phase for sample-and-hold channel 111, sampling capacitor circuit C_{s1} may sample voltage VIN. Similarly, sample-and-hold channel 111 is arranged such that, during a hold phase for sample-and-hold channel 111, sampling switch circuit S_{s1} is open and switch circuit S_{h1} is closed. Also, during the hold phase for sample-and-hold channel 111, switch circuit S_{h1} is arranged to provide signal SH_out1 to first channel 121. First channel 121 may continue processing signal SH_out1 during the subsequent sample phase. Since switch circuit S_{h1} is open, first channel 121 does not receive a new signal until the next hold phase for sample-and-hold channel 111. This way, first channel 121 can use the hold phase for sample-and-hold channel 111 and the subsequent sample phase for sample-and-hold channel 111 to process signal SH_out1 until the next sampled signal needs to be processed by first channel 121.

In a similar manner, sample-and-hold channel 112 is arranged such that, during a sample phase for sample-and-hold channel 112, sampling switch circuit S_{s2} is closed and holding switch circuit S_{h2} is open. During the sample phase for sample-and-hold channel 112, sampling capacitor circuit Cs2 may sample voltage VIN. Also, sample-and-hold channel 112 is arranged such that, during a hold phase for sample-and-hold channel 112, sampling switch circuit S_{s2} is open and holding switch circuit S_{h2} is closed. As described with regard to switch circuit S_{h1} above, second channel 122 can use the hold phase for the sample-and-hold channel 112 and the subsequent sample phase for sample-and-hold channel 112 to process signal SH_out2 until the next sample needs to be processed by second channel 122.

In one embodiment, by pipelining sample-and-hold circuit 102 in two in the manner described, the speed of sample-and-hold circuit 102 is substantially doubled, without substantially decreasing the processing time allowed for processing circuit 120. In other embodiments, sample-and-hold circuit 102 may be pipelined by more than two.

Processing circuit 120 may be interleaved such that first channel 121 and second channel 122 are substantially similar.

In one embodiment, signals VIN, SH_out1 and SH_out2 are all single-ended signals. In other embodiments, one or more of signal VIN, SH_out1 and SH_out2 are

differential signals. In another embodiment, although not shown, circuit 100 may be arranged to operate in single-ended mode if signal SE (not shown) is asserted, and to operate in differential mode if signal SE is not asserted.

FIGURE 2 illustrates a block diagram of an embodiment of circuit 200 in which the sample-and-hold circuit includes buffer circuits, and the processing circuit is an ADC circuit. Components in circuit 200 may operate in a substantially similar manner to similarly-named components in circuit 100, and may operate in a different manner in some ways. Processing circuit 220 is an interleaved ADC circuit that includes ADC bank 221 and ADC bank 222. Sample-and-hold circuit 202 further includes buffer circuits 236, 238, and 230.

In operation, buffer circuit 230 may provide signal VIN_buf from signal VIN. Buffer circuit 230 may prevent kickback noise created by the switching operation and by transient currents drawn by sampling capacitor circuits C_{s1} and C_{s2}. Similarly, buffer circuits 236 and 238 may help stop any constant or transient current drawn by processing circuit 220 that might otherwise corrupt the voltage stored in sampling capacitor circuits C_{s1} and C_{s2} respectively.

Switch circuits S_{s1} and S_{h2} are arranged to be closed if signal phi1 is high, and arranged to be open if signal phi1 is low. Conversely, switch circuits S_{s2} and S_{h1} are arranged to be closed if signal phi2 is high, and arranged to be open if signal phi2 is low. During the hold phase for switch circuit S_{h1}, the relatively large input capacitance associated with ADC bank 221 is not coupled to sampling capacitor circuit C_{s1}. Also, a break-before-make scheme may be implemented so that a short delay occurs between the time that sampling switch circuit S_{s1} turns off and the time that hold switch circuit S_{h1} turns on, and so that another short delay occurs between the time that hold switch circuit S_{h1} turns off and the time that sampling switch circuit S_{s1} turns on. Additionally, although not shown in FIGURE 2, signals phi1 and phi2 are provided from one of more clock signals CLKs.

Sample-and-hold channel 212 operates in a substantially similar manner as sample-and-hold channel 211, except than sample-and-hold channel 212 is sampling when sample-and-hold channel 211 is holding, and vice versa.

FIGURE 3 shows a timing diagram of waveforms of embodiments of signals CLKs, phi1, and phi2 from circuit 200. Waveform 360 shows an embodiment of one or more clock signals CLKs. Waveform 362 shows an embodiment of signal phi1, and waveform 364 shows an embodiment of signal phi2. For the embodiments of signals phi1 and phi2 illustrated in FIGURE 3, the period of signals phi1 and phi2 are twice the period of clock signals CLKs. Also, signal phi2 is a substantial inverse of signal phi1. When signal phi1 is high, signal VIN_buf is sampled on sampling capacitor circuit C_{s1}. When signal phi1 is low, the sampled signal is held to provide signal SH_out1. When signal phi1 changes from low to high once again, a new signal VIN_buf is sampled again. However, while new signal VIN_buf is being sampled, ADC bank 221 continues processing the old SH_out1 signal, since switch circuit S_{h1} remains open.

FIGURE 4 illustrates a block diagram of an embodiment of circuit 400 that includes a boost circuit. Circuit 400 includes sampling switch circuit S_{s1}, capacitor circuit C_{s1}, boost circuit 441, processing circuit 420, and holding switch circuit S_{h1}. In circuit 400, holding switch circuit S_{h1} includes boosted switch circuit 451 and dummy circuit 452. Components in circuit 400 may operate in a substantially similar manner to similarly-named components in circuit 200 from FIGURE 2, and may operate in a different manner in some ways.

In operation, boost circuit 441 provides boost signal Boost and another boost signal BoostB from signals CLKs, phi2, VDD, and GND. Signal BoostB is a substantial inverse of signal Boost. Signals CLKs may include one or more clock signals. Signals CLKs alternate between a low voltage that corresponds to signal GND, and a high voltage that corresponds to VDD. Signals Boost and BoostB alternate between a boosted voltage VDDB and an off voltage V_{OFF}. Boosted voltage VDDB is greater than VDD. In one embodiment, off voltage V_{OFF} is substantially similar to signal GND. In other embodiment, voltage V_{OFF} is significantly greater than signal GND. In one embodiment, GND is 0V, VDD is 1.9V, VDDB is 2.6V, and V_{OFF} is 1.0V. In other embodiments, other voltages may be employed.

Sampling switch circuit S_{s1} is arranged to couple node N1 to node N2 if signal phi1 is high. This way, when signal phi1 is high, sampling capacitor circuit C_{s1} stores a charge on to sample voltage VIN. Boosted switch circuit 451 is arranged to receive

signal Boost. Further, boosted switch circuit 451 is arranged to couple node N2 to node N3 if signal Boost corresponds to VDDB. Dummy circuit 452 is arranged to cancel charge injection when boosted switch circuit 451 is turned off. Further, dummy circuit 452 is arranged such that dummy circuit 452 is on when signal BoostB corresponds to VDDB, and such that dummy circuit 452 is off when signal BoostB corresponds to voltage V_{OFF}. In one embodiment, dummy circuit 452 operates as a capacitor when dummy circuit 452 is on, and may operate substantially as a short circuit when dummy circuit 452 is off.

FIGURE 5 shows a block diagram of an embodiment of portion 506 of circuit 400 from FIGURE 4, in which one embodiment of a hold circuit from FIGURE 4 is schematically illustrated. Components in portion 506 may operate in a substantially similar manner to similarly-named components in circuit 400, and may operate in a different manner in some ways. Similarly, signals $phi2_{BOOST}$ and $phi2b_{BOOST}$ may operate in a similar manner as described with regard to signal Boost and BoostB respectively from FIGURE 4, and may operate in a different manner in some ways. Portion 506 may further include buffer circuit 536. Processing circuit 520 may include ADC bank 521. Also, in portion 506, holding switch circuit S_{hl} includes transistors M1-M3.

Transistor M1 is arranged to operate as a boosted switch circuit responsive to signal $phi2_{BOOST}$. Transistors M2 and M3 are each arranged to operate as a dummy circuit that is responsive to signal $phi2b_{BOOST}$. More specifically, transistors M2 and M3 are each arranged to store half of the charge injection from transistor M1 when transistor M1 turns off. As shown in FIGURE 5, transistor M1 has an associated channel width W, and transistor M2 and M3 each have an associated channel width that is given by approximately W/2.

FIGURE 6 illustrates a timing diagram of waveforms of embodiments of signals CLKs, $phi2_{BOOST}$ and $phi2b_{BOOST}$ from FIGUREs 4 and 5. Waveform 660 illustrates signals CLKs, which alternate between 0V and VDD. Waveform 665 illustrates signal $phi2_{BOOST}$, which alternates between signal VDDB and signal V_{OFF}. In the embodiment shown in FIGURE 6, VDDB is significantly greater than VDD, and V_{OFF} is significantly greater than 0V. Also, waveform 667 illustrates signal $phi2b_{BOOST}$, which is a substantial inverse of signal 665.

FIGURE 7 shows a block diagram of an embodiment of portion 706 of circuit 400 from FIGURE 4, in which another embodiment of hold circuit S_{h1} from FIGURE 4 is schematically illustrated. Components in portion 706 may operate in a substantially similar manner to similarly-named components in circuit 400, and may operate in a different manner in some ways. Also, signals bgate1 and bgate2 may operate in a similar manner as described with regard to signal Boost from FIGURE 4, and may operate in a different manner in some ways. Similarly, signals bcancel1 and bcancel2 may operate in a similar manner as described with regard to signal BoostB from FIGURE 4, and may operate in a different manner in some ways. Portion 706 may further include buffer circuit 736. Processing circuit 720 may include ADC bank 721. Also, in portion 706, holding switch circuit S_{h1} includes half-switch circuit 770 and half-switch circuit 771. Half-switch circuit 770 includes transistors M4 and M5, and half-switch circuit 771 includes transistors M6 and M7.

Transistor M4 and M6 are each arranged to operate as a boosted switch circuit responsive to signals bgate1 and bgate2 respectively. Transistors M5 and M7 are each arranged to operate as a dummy circuit responsive to signals bcancel1 and bcancel2 respectively. As shown in FIGURE 7, transistors M4-M7 each have substantially the same channels widths.

FIGURE 8 illustrates a timing diagram of waveforms of embodiments of signals CLKs, bgate1, bgate2, bcancel1, and bcancel2 from FIGUREs 4 and 7. Waveform 860 illustrates signals CLKs, which alternate between 0V and VDD. Waveform 865 illustrates signals bgate1 and bgate2, which each alternate between signal VDDB and signal V_{OFF}. In the embodiment shown in FIGURE 8, VDDB is significantly greater than VDD, and V_{OFF} is significantly greater than 0V. Also, waveform 867 illustrates signals bcancel1 and bcancel2, which are each substantial inverses of signal bgate1.

FIGURE 9 shows a block diagram of circuit 900. Components in circuit 900 may operate in a substantially similar manner to similarly-named components in circuit 400, and may operate in a different manner in some ways. Circuit 900 includes sample-and-hold circuit 902 and processing circuit 920. Processing circuit 920 includes ADC bank 921 and ADC bank 922. Sample-and-hold circuit 902 includes buffer circuit 930, differential sample-and-hold channel 911 and differential sample-and-hold channel 912.

Differential sample-and-hold channel 911 includes sample-and-hold channel 913 and sample-and-hold channel 914. Differential sample-and-hold channel 912 includes sample-and-hold channel 915 and sample-and-hold channel 916. Sample-and-hold channel 913 includes switch circuit S_{s1}, sampling capacitor circuit C_{s1}, buffer circuit 936, and hold circuit S_{h1}. Sample-and-hold channel 914 includes switch circuit S_{s1n}, sampling capacitor circuit C_{s1n}, buffer circuit 937, and hold circuit S_{h1n}. Sample-and-hold channel 915 includes switch circuit S_{s2}, sampling capacitor circuit C_{s2}, buffer circuit 938, and hold circuit S_{h2}. Sample-and-hold channel 916 includes switch circuit S_{s2n}, sampling capacitor circuit C_{s2n}, buffer circuit 939, and hold circuit S_{h2n}.

In operation, buffer circuit 930 provides signal VIN_buf from signal VIN. In circuit 900, signals VIN and VIN_buf, SH_out1 and SH_out2 are differential signals. Also, differential sample-and-hold channel 911 is arranged to provide signal SH_out1 from signal VIN_buf. More specifically, sample-and-hold channel 913 is arranged to provide a first half of differential signal SH_out1 from a first half of differential signal VIN_buf, and sample-and-hold channel 914 is arranged to provide a second half of differential signal from a second half of differential signal VIN_buf. Differential sample-and-hold channel 912 is arranged to provide signal SH_out2 from signal VIN_buf in a similar manner.

FIGURE 10 schematically illustrates an embodiment of half-switch circuit 1070. Components in half-switch circuit 1070 may operate in a substantially similar manner as similarly-named components in half-switch circuit 770 of FIGURE 7, and may operate in a different manner in some ways. Half-switch circuit 1070 further includes boost circuit 1040, cross-coupled transistors 1090, inverters 1080, transistors M10-M13, and capacitors C3 and C4. Cross-coupled transistors 1090 include transistors M8 and M9.

Boost circuit 1040 is arranged to provide signal posbst from signals CLK, pwrp, and pwrn such that signal posbst has an associated voltage that is greater than a voltage that is associated signal pwrp. Signal pwrp is a high power supply signal, and signal pwrn is a low power supply signal. In one embodiment, signal pwrp corresponds to 1.9V, signal pwrn corresponds to 0V, and signal posbst corresponds to 2.6V.

Additionally, cross-coupled transistors 1090 are arranged to connect and disconnect the gates of transistors M4 and M5 from signal posbst. Transistors M10 and M11 are each arranged as a diode to provide gate oxide stress protection.

Inverters 1080 and transistors M12-M13 are arranged to provide signals trackd and trackb from signal phi2. Capacitor C3 is arranged to provide the clock timing from signal trackd to signal bgate1. Similarly, capacitor C4 is arranged to provide the clock timing from signal trackb to signal bcancel1.

FIGURE 11 schematically illustrates an embodiment of a boost switch circuit 1140. Boost switch circuit 1140 may operate in a substantially similar manner as described with regard to boost circuit 1040 from FIGURE 10, and may operate in a different manner in some ways.

The above specification, examples and data provide a description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention also resides in the claims hereinafter appended.